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REMARKS

Claims 1-15, all the claims pending in the application, stand rejected on prior art grounds. Claims 5-10 stand rejected upon informalities. Applicants herein amend the claims 1, 4, 5, and 11-13. Additionally, claims 16-20 are added herein. Additionally, Applicants herein amend the specification to correct obvious typographical errors. No new matter is being presented. Applicants respectfully traverse these rejections based on the following discussion.

I. The Information Disclosure Statement

The Office Action indicates that the Information Disclosure Statement filed on December 10, 2001 fails to comply with 37 C.F.R. §1.98(a)(3). As such, Applicants are herein submitting an English translation of the Abstract of Japanese Patent No. JP4303234 (Japanese Patent No. JP4303234 was previously submitted in the above-mentioned IDS on December 10, 2001). Moreover, Applicants respectfully request that the Examiner consider the attached prior art and make it a part of the record. While no additional fee is believed to be required, should any additional fee be necessary, the Commissioner is requested to charge Attorney's Deposit Account Number 50-0510.

II. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 5-10 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As such, Applicants have amended claim 5 (and claims 6-10 by inherency) to remove the offending language, to provide proper antecedent basis for the claimed language, and to provide clarity to the claimed language. Specifically, claim 5 has been

amended, in part, to recite, "...a counting circuit for dividing data into a plurality of groups, and for counting a difference between data to be transferred and data transferred immediately before said data to be transferred for each said group..." In view of the foregoing, the Examiner the use respectfully requested to reconsider and withdraw this rejection.

III. The Prior Art Rejections

Claims 1-3 and 5-13 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,553,445, Drapkin, et al., hereinafter referred to as "Drapkin." Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Drapkin in view of U.S. Patent No. 5,781,742, Asano, et al., hereinafter referred to as "Asano." Claims 14-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Drapkin in view of U.S. Patent No. 5,931,927, Takashima. Applicants respectfully traverse these rejections based on the following discussion.

Drapkin teaches a method and apparatus for simultaneously communicating data over a plurality of data links, such as a bus, and determines initial logic levels of data to the output on each of the plurality of data links and changes the logic levels, such as inverting the data, of at least some of the data to produce logic level adjusted data in response to determining the initial logic level of the data to reduce switching transitions of simultaneously switched output data over the plurality of data links.

Asano teaches a data transfer system that effectively reduces EMI radiation, in a device wherein EMI radiation very easily occurs, without the need for filters, etc. Asano teaches a system for transmitting data across a bus having a plurality of data lines includes a modulating circuit for modulating data so as to reduce the EMI radiation attributable to the data lines and a demodulating circuit for restoring the original data after transmission.

Takashima teaches an output device comprising in-chip data lines of an m-bit (m is an integer of eight or more) configuration for transferring m-bit data containing 1 bits and/or 0 bits, m in-chip output circuits for respectively outputting m bits on the in-chip data lines to m external output pins, decision means, provided for each of n (n is an integer of two or more) groups into which the in-chip data lines and the in-chip output circuits are divided, for deciding whether all bits on each of the n groups of data lines are to be inverted or not on the basis of m-bit data, data inversion circuits provided between the in-chip data lines and the in-chip output circuits in each of at least (n-1) groups and responsive to an output of the decision means for inverting all bits in data on the corresponding in-chip data lines, and inversion information output circuits for outputting to external output pins information indicating whether data in the (n-1) groups have been inverted or not.

However, the claimed invention, as provided in amended independent claims 1, 4, 5, and 11-13 contain features, which are patentably distinguishable from the prior art references of record. Specifically, amended claims 1, 4, 5, and 11-13 include reference to a "display device", which the Office Action (page 7, first paragraph) readily admits Drapkin does not expressly disclose. Thus, Applicants respectfully propose that they have overcome the 35 U.S.C. §102(e) rejections to claims 1-3 and 5-13. Furthermore, Takashima does not teach a display device. Thus, Applicants respectfully propose that they have overcome the 35 U.S.C. §103(a) rejections to claims 14 and 15 as well.

With regard to the rejection of claim 4, the Office Action indicates that Asano teaches a display device, which would be obvious to combine with Drapkin to teach the Applicants' claimed language. However, claim 4 has been amended to further include the distinction that, "...wherein said determination unit comprises a counting circuit adapted for counting a

difference between data to be transferred and data transferred immediately before said data to be transferred for each said group;..." which is neither taught nor suggested in Drapkin, Asano, or Takashima, or any of the other prior art references of record and/or in the application file. Additionally, claims 1, 5, and 11-13 are similarly amended with similar claimed language.

This distinction yields a significant advantage of the claimed invention, whereby, the determination unit counts the number of Transferring Data (data to be transferred) and the number of Proximate Data (data transferred immediately before the Transferring Data) for each group, determines the difference between these numbers (number of Transferring Data and number of Proximate Data), and selects a combination of inversion/non-inversion of each group based on the results of the counting (i.e., difference between the Transferring Data and Proximate Data) in order to minimize a sum total of changes of data for all the groups.

That is, the determination of the inversion/non-inversion for each group is based on both the Transferring Data (data to be transferred) and the Proximate Data (data transferred immediately before the Transferring Data). Thus, at the time of starting the data transfer, Electro-Magnetic Interference (EMI) can be suppressed at the first data. Conversely, in Drapkin the counter 306 merely counts the number of logic "1s" that are present in the bit group and outputs the total number of "1s" as a number of initial data logic levels 322. Hence, there is no accounting for previously transferred data (Proximate Data) in Drapkin. Thus, the claimed invention is able to achieve a greater reduction in the EMI associated with the data transfer than the noise/interface reduction in Drapkin because of this Proximate Data accountability.

Furthermore, according to the Applicants' invention based on the results of counting carried out by the signal change detectors 31A and 31B, the statistics analyzer 32 performs analysis for determination as to whether data should be inverted or not, for each of the groups.

Based on the results of counting carried out by the signal change detectors 31A and 31B, the statistics analyzer 32 examines the combinations of the following four cases: (1) neither data of the groups A and B is inverted; (2) the data of the group B is inverted while the data of the group A is not; (3) the data of the group A is inverted while the data of the group B is not; and (4) both data of the groups A and B is inverted. While Drapkin teaches inverting groups of data, these specific features are not taught or suggested in Drapkin.

Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these rejections.

IV. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-15, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,

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DATA TRANSFER SYSTEM

Patent number: JP4303234
Publication date: 1992-10-27
Inventor: KOMORI NOBUFUMI
Applicant: MITSUBISHI ELECTRIC CORP
Classification:
- International: G06F5/00; G06F13/38
- european:
Application number: JP19910091598 19910329
Priority number(s):

Abstract of **JP4303234**

PURPOSE:To transfer data with a high reliability without reducing the effective transfer rate of multibit parallel data where simultaneous switching noise occurs.
CONSTITUTION:A bit change detecting circuit 1 compares data outputted at present and data to be next outputted with each other with one bit as the unit to detect whether the bit variation is larger than a set value or not, and a bit pattern conversion signal which is significant in the case of the bit variation larger than the set value is outputted. If the bit pattern conversion signal is significant, a bit pattern converting circuit 2 inverts all bits of data to be next outputted to output the bit pattern of less bit variation; but otherwise, the circuit 2 outputs this data as it is. The one-bit of bit pattern conversion signal is added to this output, and it is transferred. The transfer destination fetches transfer data including the one-bit of bit pattern conversion signal; and if the bit pattern conversion signal is significant, all bits are internally inverted to restore the original data.